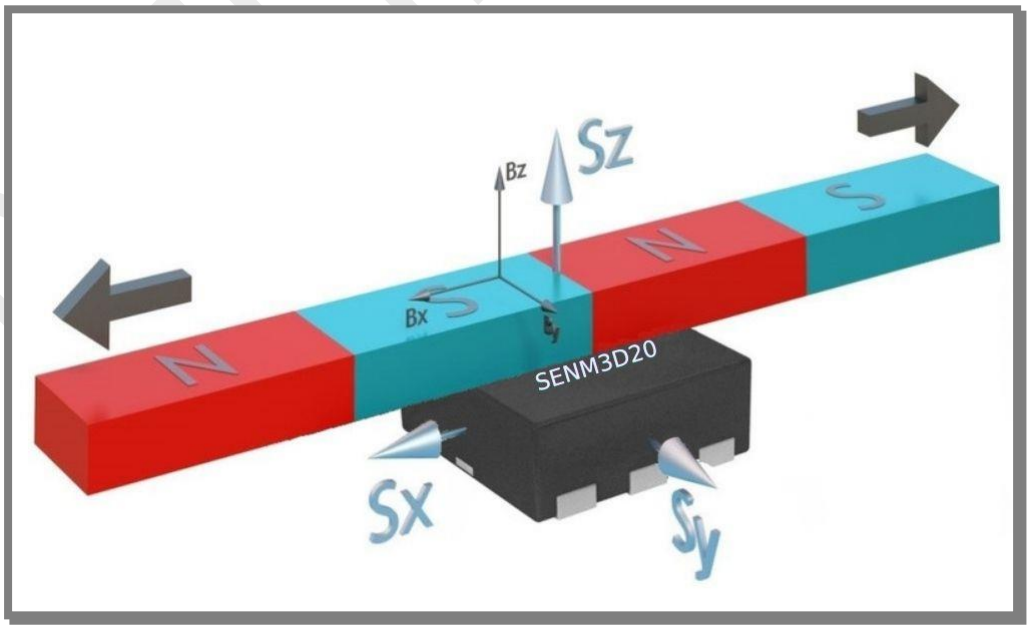
SENSORS

Preliminary datasheet Rev.1
SENIS® AnyAxis Sensor SENM3D20

3Axis hall sensor

1. DESCRIPTION:

AnyAxis, a successor stemming from the established SENM3Dx is designed to enhance magnetic field sensing capabilities with a range of advanced features. Three-axis Hall sensor, AnyAxis enables simultaneous measurement of magnetic field components at a single point. The sensor supports four programmable dynamic ranges) providing adaptability to varied operational needs and flexibility with three acquisition modes. AnyAxis offers programmable interrupt modes and with an embedded LDO regulator, the sensor ensures flexibility and efficiency. High-speed 16-bit ADC of AnyAxis facilitates swift and accurate data acquisition. An 8-bit mode is available for even faster data readout. EEPROM for internal calibration and device address programmability through EEPROM memory for multiple-devices configuration. AnyAxis offers a practical and reliable solution for magnetic field sensing needs, emphasizing accuracy and adaptability across diverse applications.



2. KEY FEATURES

ANYAXIS is a three axis HALL sensor IC with these following features:

- Three axis Hall sensor (X, Y and Z)
- Four programmable dynamic ranges +/- 12.5mT / 50mT / 100mT and 200mT.
- Built-in temperature sensor. Temperature readout on demand by the host.
- Three acquisition modes: On demand, slow (programmable refresh rate) or continuous.
- Programmable interrupt modes: Absolute or relative threshold, signed or unsigned.
- Large range single power supply (2.5V to 5V) with embedded LDO regulator.
- Temperature range: -40C to 150C, with degraded performance above 125C.
- Serial interface: I2C FM+ Device address programmable through EEPROM memory for multiple-devices configuration.
- 16-bit ADC with 25 Ks/s refresh rate (1 axis) or 8.33 Ks/s (3 axis). An 8-bit mode for faster data readout.
- EEPROM memory for internal calibration: oscillator, bandgap and temperature sensor. Sensor offset, temperature coefficient compensation and system configuration.
- Process X-FAB XP018

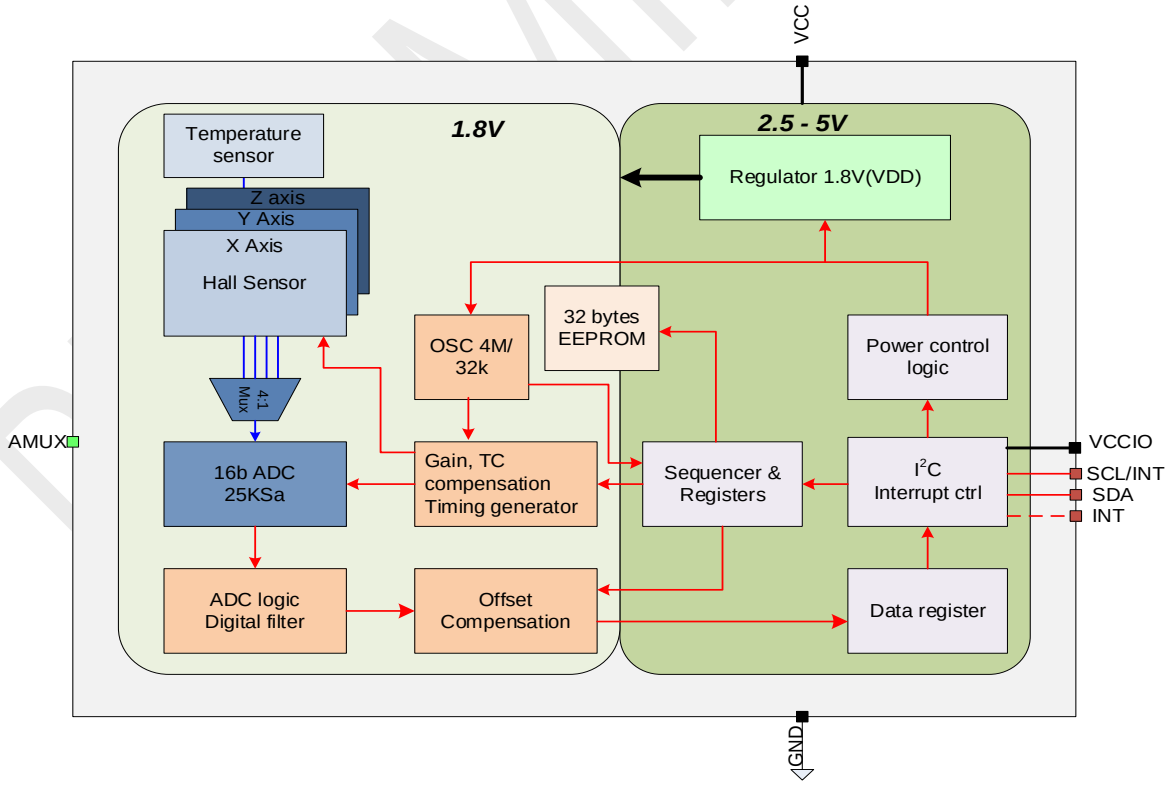


Figure 1 - ANYAXIS top level diagram

Contents:

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3. ELECTRICAL PARAMETERS AND SENSOR PERFORMANCE

Unless otherwise noted, the given specifications and characteristics are typical values and apply for room temperature (23°C) and after a device warm up time of 15 minutes and VCC=5 V.

3.1. Absolute maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage	VCC	-0.7	7	V
All outputs		-0.3	7	V
Storage Temperature	TSTG	-50	150	°C
Operating Temperature Range	Tamb	-40	150	°C
Lead Temperature (soldering, 10 seconds)	TL		220	°C
ESD HBM Protection	Vesd		2.0	kV

Table 1: I2C Absolute maximum ratings.

3.2. Electrical characteristics

3.2.1. Power supply voltages and current

Parameter description / test conditions	Min	Typ	Max	Unit
Power supply voltage VCC	2.5		4.2	V
Active mode current VCC			3	mA
Idle mode current			10	uA
Sleep mode current			10	nA
Power on reset threshold			2.4	V
Power on reset hysteresis		250		mV
Power on delay from power up			30	us
Power on delay from idle			1u	mV
Power on delay from sleep			30	us

Table 2: Voltages and current

3.2.2. Sensor performance

Parameter description / test conditions	Min	Typ	Max	Unit
Magnetic field sensitivity range (4 selectable ranges)	12.5m		200m	T
Magnetic field fine sensitivity programming resolution (in any range)		0.4		% of S
Magnetic sensitivity temperature drift (-40c to 150C)	-1		1	% of S
Magnetic sensitivity temperature compensation range	0		2800	ppm/C of S
Magnetic sensitivity temperature compensation resolution		175		ppm/C of S
Magnetic offset (16-bits mode)			0.5	% of S
Magnetic offset drift (16-bits mode)			0.02	% of S/ C
RTI Noise			200u	T_{RMS}
Output bandwidth			12.5	kHz
Temperature resolution		25m		C/Cnt

Table 3: I2C performance characteristics

3.3 Magnetic performances

Non-linearity of the sensor signal is < 1% for all axis over the full signal range.

Sensitivity to DC magnetic field	Value for specified axis		
	Bx	**By**	**Bz**
Range	Sensitivity [V/T]		
15 mT	TBD	TBD	TBD
30 mT	TBD	TBD	TBD
300 mT	TBD	TBD	TBD
3000 mT	TBD	TBD	TBD
Range	Sensitivity [ADC cnts/T]		
15 mT	TBD	TBD	TBD
30 mT	TBD	TBD	TBD
300 mT	TBD	TBD	TBD
3000 mT	TBD	TBD	TBD

Table 4: Sensor sensitivity

Zero Magnetic Field Offsets	Value for specified axis		
	Bx	**By**	**Bz**
Range	Corresponding Digital Output [ADC cnts]		
15 mT	TBD	TBD	TBD
30 mT	TBD	TBD	TBD
300 mT	TBD	TBD	TBD
3000 mT	TBD	TBD	TBD
Range	Corresponding Magnetic Field [mT]		
15 mT	TBD	TBD	TBD
30 mT	TBD	TBD	TBD
300 mT	TBD	TBD	TBD
3000 mT	TBD	TBD	TBD

Table 5: Uncorrected zero magnetic field offsets

Noise Spectral Densities	Value for specified axis		
	Bx	**By**	**Bz**
Range	Voltage Noise NSD @ f > 10 Hz (white noise), [µV/$\sqrt{Hz}$]		
15 mT	16.0	19.0	17.0
30 mT	9.2	9.3	8.5
300 mT	1.3	1.3	1.2
3000 mT	*0.90*	*0.91*	*0.85*
Range	Corresponding Magnetic Field NSD @ f > 10 Hz (white noise), [µT/$\sqrt{Hz}$]		
15 mT	*0.90*	*0.91*	*0.85*
30 mT	*0.13*	*0.14*	*0.15*
300 mT	*0.19*	*0.20*	*0.27*
3000 mT	*1.50*	*1.52*	*1.60*

Table 6: Input referred, equivalent white noise specification of the sensor

4. FUNCTIONAL DESCRIPTION

4.1. Device modes of operation

There are 3 modes of operations as described in the following table, drawing different amount of power from the power supply:

- On Demand mode.
- Slow mode.
- Continuous mode.

Mode of operation	**Power state**	**Power supply behavior**	**Oscillator behavior**
On demand	Sleep -> Active -> Sleep	1.8V LDO is disabled. I2C interface powered through main power supplies VCC/VCCIO. (*Note 1*)	Off (not powered)
Slow	Idle -> Active -> Idle	1.8V LDO is enabled, and powers the oscillator and a timer to wake up the device at regular intervals. I2C interface powered through main power supplies VCC/VCCIO. (Note 1)	On 32 kHz output, not calibrated. (+/- 5%)
Continuous	Active	1.8V LDO is enabled, and powers the entire device. I2C interface powered through main power supplies VCC/VCCIO.	On 4 MHz output, calibrated

Table 7: Modes of operation

Once the conversion period is complete, the new conversion data are stored into registers and compared to the interrupt threshold of the enabled sensors and the interrupt line is eventually activated low to indicate a valid interrupt condition. At the same time the data validity flags inside the **STATUS** register are set. From that point the device goes back to Sleep/Idle, and the host can read the data at any time. If a new conversion cycle starts the current data will be lost. The Data validity flags are cleared when entering Active power state.

*Note 1: When going out of Idle/Sleep power state due to a host request or an internal wake-up event, the device goes to Active power state. The internal resources are enabled, and the conversion sequence is performed after a settling period whose duration depends on the mode of operation (going out of sleep power state takes longer than going out of idle power state). Depending on the number of sensors enabled through the register **SENSOR_CFG**, and the number of averaged samples defined by the **FILTER_CFG** register, from 1 to 4*128 = 512 conversion cycles are executed.*

4.1.1. On demand mode

This is the least power consuming mode, in which the device consumes less than 10nA while in sleep power state. The duration of the active state depends on the **FILTER_CFG** register where the number of average samples are defined and on the **SENSOR_CFG** register where individual sensors (X, Y, Z and Temperature) are enabled.

The sequencing of this mode is:

- The IC wakes up from sleep with the I2C command **CMD_WAKEUP**.
- The 1.8V LDO and 4MHz oscillator are turned ON. The device will take 30us to turn itself on before any magnetic field measurement can start.
- The magnetic field measurement starts according to **SENSOR_CFG** and **SENSOR_CFG** registers and the corresponding ADC data are saved into the appropriate shadow registers.
- Go back to Sleep power state by shutting down the power supply to the 1.8V section.

4.1.2. Slow mode

In this mode, the device consumes less than 10uA while in idle power state. The duration of the active state depends on the FILTER_CFG register where the number of average samples is defined, and on the SENSOR_CFG register where individual sensors (X, Y, Z and Temperature) are enabled. The 1.8V LDO remains active during Idle.

The sequencing of this mode is:

- The device wakes up from Idle power state every time an internal timer running on an un-calibrated 32KHz oscillator reaches the delay defined in the **READOUT_CFG** register.
- The oscillator frequency is increased from 32KHz to 4MHz.
- The magnetic field measurement starts according to **SENSOR_CFG** and **SENSOR_CFG** registers and the corresponding ADC data are saved into the appropriate shadow registers.
- Go back to Idle power state by reducing the oscillator frequency to 32kHz and switching Off the analog sensors.

*Note: If the **SENSOR_CFG** and **FILTER_CFG** registers settings yields a conversion time larger than the delay defined by the **READOUT_CFG** register, then the device will never go to Idle power state and will operate in Continuous mode.*

4.1.3 Continuous mode

The IC remains at high power and operates at its maximum conversion rate.

The sequencing of this mode is:

- Measure the magnetic field continuously according to **SENSOR_CFG** and **FILTER_CFG** registers and save the ADC data into the appropriate shadow registers. The data validity flags of the sensors enabled through the **SENSOR_CFG** register remain set after the first conversion.

*Note: The data update rate is defined by the **SENSOR_CFG** and **FILTER_CFG** registers with a maximum of 25 Ksamples/s if one sensor is enabled and one sample is taken.*

4.2 Magnetic (Hall effect) sensor circuit

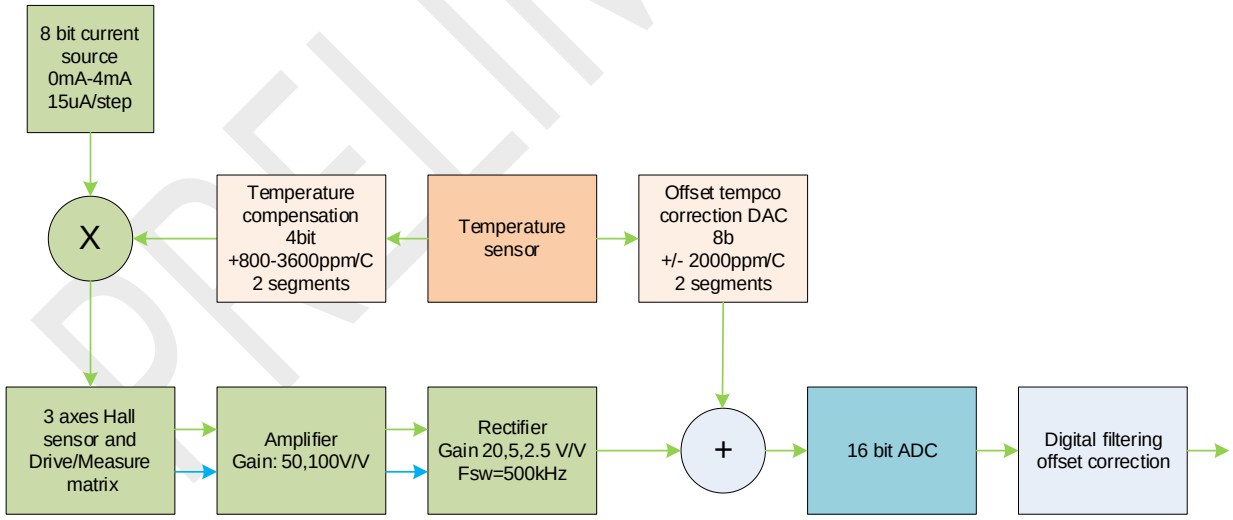

Figure 2: Hall sensor

Three HALL sensors for different magnetic axes are used in this IC (X, Y and Z planes).

- The gain of the Hall sensor is controlled by the **x_GAIN_CAL** register through the adjustment of the bias current of the Hall sensor.
- A 3 to 1 analog multiplexer connects the 3 sensors to a common analog processing circuit and a 16-bit ADC. An additional mux input will allow the conversion of the Temperature sensor voltage, for internal temperature compensation and eventual host readout.
- The Hall sensor uses 4 phase rectification to measure the magnetic field. Each of the measurement cycle lasts 4us.
- The ADC is a 16 ΔΣ with an oversampling ratio of 32. The digital filter is a 3rd order decimator followed by an averaging circuit. The number of samples "nb_sample" defined by the register **FILTER_CFG** are summed together, and the result is divided by the number of samples.
- Each measurement sample (include 16bit ADC) requires 2*32+"nb_sample" *32 +4 clock cycles (4MHz). A smaller number of samples allow a faster conversion time at the expense of a higher noise figure. On the other hand, a larger number of samples increases the conversion time but reduces the noise figure.
-
- The sensor configuration register allows the user to define the sensitivity of the IC.
- The range can be selected from 12.5mT, 50mT, 100mT and 200mT respectively.
- Each sensor can be enabled/disabled individually.

To configure the sensors six registers are used:

SENSOR_CFG selects sensitivity, magnetic axes, and mode of operation.

READOUT_CFG selects update rate in slow mode.

FILTER_CFG selects digital filter setting and interrupt signal generation mode.

INT_THRES_X, **INT_THRES_Y** and **INT_THRES_Z** define the comparison threshold for interrupt generation.

Filter setting (FILTER_CFG)	# Sample	Noise RTI (uTrms)	1 Sensor (sample/s)	3 Sensors (sample/s)
0	1	141	25000	8333
1	2	100	20833	6944
2	4	71	13889	4630
3	8	50	7813	2604
4	16	35	4032	1344
5	32	25	2016	672
6	64	18	1000	333
7	128	13	496	165

Table 8: Noise figure / conversion rate vs number of samples

4.2.1 Calibration

The calibration parameters are saved in the EEPROM memory. Upon reset, and if the checksum of the factory page is corrected, the EEPROM content will be copied into the main register. If the checksum is wrong, the default value will be used.

4.2.2. Temperature calibration

The reading from temperature sensor will be added with TEMP_CAL (16bits) to yield 0x8000 at 30 degree C. The temperature can be determined by the following equations:
T_{IC} = <DATATH: DATATL> /40 -789 (16-bit readout mode)
T_{IC} = <DATAT>*6.4 -789 (8-bit readout mode)

4.2.3 Gain calibration

Gain variation including the temperature coefficient is compensated through analog circuitry in the Hall sensor measurement.

- The gain (sensitivity) calibration is done through the ***_GAIN_CAL** registers, which control the bias current driven through the HALL sensor. The current range of the calibration is from minimum 16uA to a maximum of 4.08mA. The gain is calibrated in factory at the maximum sensitivity (12.5mT), and compensation for gain setting will be scaled accordingly by shifting the register contents, so no additional calibration is required.
- The gain temperature coefficient calibration is done through ***_GAIN_TC_CAL** registers, which control the temperature coefficient of the bias current in two segments. The first segment (4 LSBs) is for temperatures below 30C, while the second segment (4 MSBs) compensates for temperature greater than 30C. The TC compensation range is from 800ppm to 3000ppm in 15 steps. The same compensation parameter will be used for all gain settings.

4.2.4 Output offset calibration

- Offset calibration is done through the digital section by subtracting the content of registers ***_OFF_CAL** of the readout result. The offset temperature coefficient is compensated through analog injection before the ADC, using the register.
  The offset calibration is done at the maximum sensitivity (12.5 mT), and the offset will be scaled down for other gain.

  $Output_{(digital)} = ADC + ***\_OFF\_CAL**32/<scale\_factor^{*}>$.

- The TC offset calibration is done through a temperature compensation circuit and a DAC to control the scale of the correction. Two registers are provided for temperatures smaller than 30C (***_OFF_TC_CAL1**) and temperature greater than 30C (***_OFF_TC_CAL2**).

  $Output_{(analog)} = sensor\ voltage + ***\_OFF\_TC\_CAL(1,2)**16/<scale\_factor^{*}>$.

4.2.5. Clock calibration

- The register CLOCK_CAL is used to calibrate the clock frequency to 4MHz (Temperature 30 degree C).

4.3. Main digital section

The main digital section is composed of the main sequencer, ADC back-end interface, I2C interface and associated data register, and EEPROM memory.

Depending on if the associated resources are needed in Sleep power state (where 1.8V power supply is not available), individual functional blocks are either located in the 1.8V power domain, or in the external power supply domain VCC.
In Idle power state (in-between conversions in slow mode of operation) the functional blocks inside the 1.8V power domain are powered and keeps their active state, and the clock source remains active at low frequency (32KHz).

Note: Functional blocks inside the VCC power domain are always ON. Some will be sequenced by the 32KHz oscillator while others will be sequenced by the I2C SCL clock.

4.3.1. Main sequencer

Power domain: VCC.
Clock domain: Local oscillator.

The purpose of the main sequencer is to sequence all the device operations, both in Sleep/Idle power state to wake-up the device when required, and in Active power state to control the various phases required to process the active Hall sensor signal all the way to ADC conversion, and interrupt monitoring.

From the moment the device goes out of Sleep/Idle power mode for conversion to the moment it goes back to this power mode again, a suite of tasks is performed as shown in the following timing diagram.

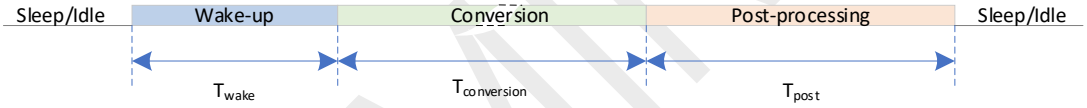

Figure 3: High-level sequencing

5. Wake-up: the processing is different for Idle or Sleep.
    a. Sleep power state: The 1.8V regulator is started, followed by the 4MHz oscillator and the internal bias sources. Then the main digital section starts.
    b. Idle power state: oscillator frequency is switched from 32 KHz to 4 MHz, the internal bias sources are turned ON. The main digital section keeps its current state.
6. Conversion process: one by one, the sensors enabled through the **SENSOR_CFG** register are processed by the ADC sub-module. If multiple samples are accumulated, then the conversion process is performed as many times as necessary.
7. Post-processing: the conversion data are transferred to the I2C power domain, ready for readout. The Data ready flags inside the **STATUS** register are updated, and the data are compared to the internally calculated interrupt threshold. If a valid condition is found the external interrupt line is activated.

For the continuous mode, in which the device does not go to Idle or Sleep power mode between conversions, the task 'wake-up' is bypassed.

4.3.2. ADC Back-end interface

Power domain: 1.8V.
Clock domain: Local oscillator.

The ADC back-end interface includes the Sigma-Delta back-end filters, which will accumulate as many samples as specified by the **FILTER_CFG** register. The resulting 16-bit data (16 MSBs) will be offset compensated (see below).

4.3.3. Interrupt

The interrupt feature allows the host controller to be notified when the signal level of one of the X/Y/Z hall-effect sensor sensors behaves as defined by the interrupt control register INT_CFG. Depending on the configuration bit set inside the DEVICE_CFG memory cell inside the EEPROM memory, the interrupt line can be assigned to a dedicated INT pad or be shared with the I2C SCL line. In either case the interrupt event is signaled by a 10 us low-level pulse.

Two Interrupt modes are available:

- An absolute mode in which the pre-defined threshold (registers *_INT_THRESH) is compared directly to the X/Y/Z sensor ADC data.
- A Relative mode where the pre-defined threshold is added as a signed number to the previous data sample. If the threshold would trigger an overflow/underflow when added to the signal level, then the threshold will be set to <max positive value>/<min positive value>.

For both modes, and in case the interrupt is programmed as signed, the threshold is a signed number, and only signal level above a positive level (positive threshold) or below a negative level (negative threshold) will generate an interrupt event. For the unsigned configuration the unsigned threshold is compared to the absolute value of the data sample.

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The following table shows how the internal threshold is calculated depending on the current mode of operation.

Mode	Signed	Unsigned
Absolute	INT_..._THRESH x 2^9 compared to <conversion data>	INT_..._THRESH x 2^8 compared to |<conversion data>|
Relative	<previous conversion data> + INT_..._THRESH x 2^9 compared to <conversion data>	|<previous conversion data>| + INT_..._THRESH x 2^8 compared to |<conversion data>|

Table 9: Interrupt threshold calculation

4.3.4. EEPROM memory

Power domain: VCC and 1.8V. In Sleep power state the VCC power supply will be disconnected while the 1.8V is not available.
Clock domain: Local oscillator.

The non-volatile memory is built around a 32 x 8 EEPROM IP. It can be programmed once the device is configured into an 'EEPROM access mode' through an I2C command. From that point the EEPROM shadow registers accessible inside the I2C memory map can be programmed into the EEPROM memory, one page at a time (Factory and user page). In case of the factory page, and if the lock bit is set, the associated shadow registers cannot be modified anymore.
Another command will transfer the EEPROM contents inside the EEPROM shadow registers.

The EEPROM includes 2 pages, each associated with a checksum and a lock bit that prevents any further write access once set.

1. The factory page contains calibration data (Oscillator frequency trimming; offset, gain calibration and 2nd order temperature coefficients for the 3 sensitivity levels of X/Y/Z Hall-effect sensors; offset calibration for the temperature sensor).
   It also contains Company / Factory ID information.
2. The user page contains device configuration parameters, such as I2C device address and physical interrupt handling, as well as the value of the device configuration registers, to allow a device operation in a configuration without a Host controller.

Two bytes of user data can be used to store any information relevant to the product.

The following table shows EEPROM memory.

Byte #	Name	Meaning
	User Pages	Calibrate and configure at factory
0	**SENSOR_CFG**	Sensor configuration
1	**READOUT_CFG**	Read out configuration
2	**FILTER_CFG**	Filter Configuration
3	**X_INT_ THRES**	**X** sensor threshold (x256)
4	**Y_INT_THRES**	**Y** sensor threshold (x256)
5	**Z_INT_THRES**	**Z** sensor threshold (x256)
6	**DEV_CFG**	IC2 device address configuration / Interrupt pad configuration
7	**USER_DATA1**	Can be used to store product information.
8	**USER_DATA2**	The bit 7 of USER_DATA2 is used as a lock bit for the User page.
9	**CHECKSUM_USER**	Checksum. Sum of bytes [8:0]-1
	Factory page	
10	**TEMP_CAL0**	Temperature calibration low byte
11	**TEMP_CAL1**	Temperature calibration high byte
12	**X_GAIN_CAL**	X-sensor gain trim (Bias DAC)
13	**X_GAIN_TC_CAL**	X-sensor gain TC trim (2 segments)
14	**Y_GAIN_CAL**	Y-sensor gain trim (Bias DAC)
15	**Y_GAIN_TC_CAL**	Y-sensor gain TC trim (2 segments)
16	**Z_GAIN_CAL**	Z-sensor gain trim (Bias DAC)
17	**Z_GAIN_TC_CAL**	Z-sensor gain TC trim (2 segments)
18	**X_OFF_CAL**	X-sensor offset
19	**X_OFF_TC_CAL1**	X-sensor offset TC trim 1st segment
20	**X_OFF_TC_CAL2**	X-sensor offset TC trim 2nd segment
21	**Y_OFF_CAL**	Y-sensor offset
22	**Y_OFF_TC_CAL1**	Y-sensor offset TC trim 1st segment
23	**Y_OFF_TC_CAL2**	Y-sensor offset TC trim 2nd segment
24	**Z_OFF_CAL**	Z-sensor offset
25	**Z_OFF_TC_CAL1**	Z-sensor offset TC trim 1st segment
26	**Z_OFF_TC_CAL2**	Z-sensor offset TC trim 2nd segment
27	**TC_CAL**	Temperature compensation calibration
28	**CLOCK_CAL**	Clock 4MHz calibration
29	**DEVICE_ID1**	Can be used to store lot and wafer reference number.
30	**DEVICE_ID2**	The bit 7 of DEVICE_ID2 is used as a lock bit for the User page.
31	**CHECKSUM_FACTORY**	Checksum. Sum of bytes [30:10]-1

Table 10: EEPROM memory map

4.4. Communication interface

Power domain: VCC.
Clock domain: I2C SCL clock.

The communication interface allows the external Host to monitor and control the device status and is an I2C slave port.

The I2C device address can be selected from 16 pre-defined values through the DEVICE_CFG memory cell inside the EEPROM memory. When changing the shadow register contents, the host must keep track of the current device address selection to perform valid I2C access.

4.4.1. I2C register map

The following section details the register map. They can be accessed through I2C for Read and/or write depending on the address.

4.4.1.1. Readout registers

Those registers are used to transmit conversion and status data to the host. The conversion data will be updated when the associated data valid flag inside the STATUS register is activated and will stay valid until the beginning of the next acquisition, at which point the data valid flag will be cleared.
In the continuous mode of operation, the data validity flags will be set as valid after the 1st conversion cycle and stay valid.

The following table shows readout registers.

Register ID	Add	Mode	Bit	Meaning
STATUS	0x00	R	0	1 = EEPROM factory parameters checksum valid
			1	1 = X sensor Data register valid
			2	1 = Y sensor Data register valid
			3	1 = Z sensor Data register valid
			4	1 = Temperature sensor Data register valid
			5	I2C command status 1 = Command processing underway. 0 = No active commands.
			7:6	Reserved
DATA_XH	0x01	R	7:0	X sensor conversion data (MSB) *(Note 4)*
DATA_XL	0x02	R	7:0	X sensor conversion data (LSB)
DATA_YH	0x03	R	7:0	Y sensor conversion data (MSB)
DATA_YL	0x04	R	7:0	Y sensor conversion data (LSB)
DATA_ZH	0x05	R	7:0	Z sensor conversion data (MSB)
DATA_ZL	0x06	R	7:0	Z sensor conversion data (LSB)
DATA_TH	0x07	R	7:0	Temperature sensor conversion data (MSB)
DATA_TL	0x08	R	7:0	Temperature sensor conversion data (LSB)
DATA_X	0x09	R	7:0	X sensor conversion data 8bits
DATA_Y	0x0a	R	7:0	Y sensor conversion data 8bits
DATA_Z	0x0b	R	7:0	Z sensor conversion data 8bits
DATA_T	0x0c	R	7:0	Temperature sensor conversion data 8bits

Table 11: Readout registers map

4.4.1.2. EEPROM shadow registers

The EEPROM shadow registers are loaded from the EEPROM memory at initial start-up if the corresponding page (User or Factory page) is associated with a valid checksum. If the checksum of a given page is not valid, then the default register values are used.
If any shadow register is updated through an I2C write access, the new value will be used for internal processing.
The shadow registers keep their value when exiting Sleep/Idle power state.

Upon host request through an I2C command (see below) the shadow register associated with a given page (Factory or user page) can be programmed into the corresponding EEPROM locations. It is the host responsibility to calculate the proper checksum and decide whether to lock the page through the lock bit.
Another I2C command allows the host to read the EEPROM (both factory and user page).

The table below illustrates how EEPROM values configure the sensor's operational settings.

Register ID	Add	Mode	Bit	Meaning	Default	
SENSOR_CFG	0x10	R/W	1:0	Sensor sensitivity 00 = 12.5 mT 01 = 50 mT 10 = 100 mT 11 = 200 mT		User page EEPROM shadow register
			2	1 = X sensor enabled		
			3	1 = Y sensor enabled		
			4	1 = Z sensor enabled		
			5	1 = Temperature sensor enabled. Can be disabled only if all 3 sensors X, Y and Z are disabled.		
			7:6	Mode of operation 00 = On demand 01 = Slow (update rate defined by bits 6-1 of register READOUT_CFG) 1X = Fast (continuous). Update rate depends on number of sensors enabled including temperature.		
READOUT_CFG	0x11	R/W	0	Readout data width 0 = 16 bits 1 = 8 bits (the LSBs are truncated; this applies to the temperature reading as well)		
			6:1	Slow readout update rate = 640 / (1+READOUT_CFG[6-1]) s/s (Range from 10 s/s to 640 s/s)		
			7	1= I2C continuous data readout. 0 = I2C user-selected readout		
FILTER_CFG	0x12	R/W	2:0	Number of samples used for averaging. (see table 1) 0-7 -> 1, 2, 4, 8, 16, 32, 64 and 128		
			3	Interrupt mode. 0 = Absolute mode. 1 = Relative mode.		
			4	Interrupt signed mode. 0 = Unsigned mode. 1 = Signed mode.		
			7:5	Reserved		
INT_X_THRES	0x13	R/W	7:0	X sensor interrupt threshold (Note 1 below)		
INT_Y_THRES	0x14	R/W	7:0	Y sensor interrupt threshold (Note 1 below)		
INT_Z_THRES	0x15	R/W	7:0	Z sensor interrupt threshold (Note 1 below)		
DEV_CFG	0x16	R/W	1:0	I2C device address 00 = 0x00 01 = 0x01 10 = 0x02 11 = 0x03		
			2	Interrupt output 0 = the interrupt is routed to the dedicated INT pin 1= the interrupt is generated as a low pulse on the I2C SCL line.		
			7:3	Reserved		
USER_DATA_1	0x17	R/W		User data		
USER_DATA_2	0x18	R/W				
CHECKSUM_USER	0x19	R/W		Reserved		
TEMP_CAL0	0x1a	R/W	7:0	Temperature sensor offset calibration (LSB)		Factory

Register ID	Add	Mode	Bit	Meaning	Default	
TEMP_CAL1	0x1b	R/W	7:0	Temperature sensor offset calibration (MSB)		page EEPROM shadow registers (Note 2)
X_GAIN_CAL	0x1c	R/W	7:0	X sensor gain calibration		
X_GAIN_TC_CAL	0x1d	R/W	3:0	X sensor gain temperature calibration 1st segment		
			7:4	X sensor offset temperature calibration 2nd segment		
Y_GAIN_CAL_	0x1e	R/W	7:0	Y sensor gain calibration		
Y_GAIN_TC_CAL	0x1f	R/W	3:0	Y sensor gain temperature calibration 1st segment		
			7:4	Y sensor gain temperature calibration 2nd c segment		
Z_GAIN_CAL	0x20	R/W	7:0	Z sensor gain calibration		
Z_GAIN_TC_CAL	0x21	R/W	3:0	Z sensor gain temperature calibration 1st segment		
			7:4	Z sensor gain temperature calibration 2nd segment		
X_OFF_CAL	0x22	R/W	7:0	X sensor offset calibration		
X_OFF_TC_CAL1	0x23	R/W		X sensor offset temperature calibration 1st segment		
X_OFF_TC_CAL2	0x24	R/W	3:0	X sensor offset temperature calibration 2nd segment		
Y_OFF_CAL_	0x25	R/W	7:0	Y sensor offset		
Y_OFF_TC_CAL1	0x26	R/W		Y sensor offset temperature calibration 1st segment		
Y_OFF_TC_CAL2	0x27	R/W	3:0	Y sensor offset temperature calibration 2nd segment		
Z_OFF_CAL	0x28	R/W	7:0	Z sensor offset		
Z_OFF_TC_CAL1	0x29	R/W		Z sensor offset temperature calibration 1st segment		
Z_OFF_TC_CAL2	0x2a	R/W	3:0	Z sensor offset temperature calibration 2nd segment		
TC_CAL	0x2b	R/W		Temperature compensation calibration		
CLOCK_CAL	0x2c	R/W		Calibrate clock to 4 MHz		
DEVICE_ID1	0x2d	R/W		Factory data		
DEVICE_ID2	0x2e	R/W				
CHECKSUM_FACTORY	0x2f	R/W		Reserved		

Table 12: EEPROM Shadow registers map

***Note 1**: The interrupt threshold used internally is calculated as defined in section 4.3.3**Error! Reference source not found.** above.*
***Note 2**: If the factory page lock bit is set, those shadow registers cannot be modified anymore.*

3.4.1.3 Test registers

They are used to configure the device into test mode for design validation and production testing.

Register ID	Add	Mode	Bit	Meaning	Default
TEST1	0x30	R/W	7:0	Reserved	
TEST2	0x31	R/W	7:0	Reserved	

Table 13: Test registers map

4.4.2. I2C commands

When the host sends an I2C command, it issues a write at the address of the command. The first data byte must be equal to the bitwise logic inversion of the command byte, and any additional byte is disregarded A flag in the STATUS register will be set to indicate that a command is being processed, and cleared once the processing of the command is complete.

Register ID	Add	Mode	Bit	Meaning
CMD_WAKEUP	0xf0	R/W	7:0	Initiate an On-demand acquisition.
CMD_EE_ACCESS	0xf1	R/W	7:0	Configure the device so the host can write into the EEPROM shadow registers, program the EEPROM and read back the EEPROM contents into the shadow registers.
CMD_EE_PROG_USER	0xf2	R/W	7:0	The contents of the EEPROM shadow registers are written into the EEPROM memory space (user page). This command will apply only if the user page lock bit is not set.
CMD_EE_PROG_FACTORY	0xf3	R/W	7:0	The contents of the EEPROM shadow registers are written into the EEPROM memory space (Factory page). This command will apply only if the factory page lock bit is not set.
CMD_EE_READ	0xf4	R/W	7:0	READ the EEPROM contents and update the EEPROM shadow registers accordingly (both user and factory page).
CMD_OPER	0xf5	R/W	7:0	Exit the EEPROM access mode and go back to normal operation. The EEPROM shadow registers are loaded with the current EEPROM contents.

Table 14: I2C command map.

5. MECHANICAL

5.1. Pin function description and position (I2C interface)

Pin-out for DFN-8 package.

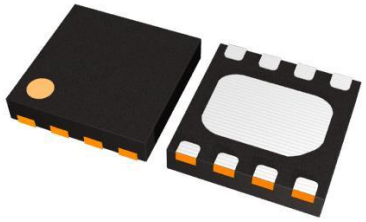

Figure 4: DFN-8 Illustration

Pin #	Symbol	Type	Description	Bonded to package
1	**SCL**	Digital Input PU[1]	I2C clock input	Yes
2	**GND**	Ground	Ground.	
3	**GND**	Ground	Ground.	
4	**INT**	Digital Output	Interrupt dedicated output.	
5	**VCCIO**	Power	Powers the digital I/Os. Can be connected to VCC if compatible with the I2C host controller.	
6	**VCC**	Power	Power (2.5V-5V) Should be forced to 5V for EEPROM programming	
7	**GND**	Ground	Ground.	
8	**SDA**	Digital Inout PU[1] OD[2]	I2C data.	
-	**AMUX**	Analog Output	Test pad to monitor internal voltages in Test/Debug mode.	No

Table 15: Pin list (DFN8)

(1) PD means weak internal Pulldown; PU means weak internal Pullup.
(2) OD means Open-Drain.

Pin-out for DFN-6 package.

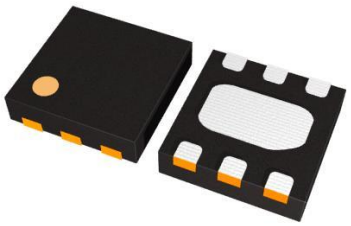

Figure 5: DFN-6 Illustration

Pin #	Symbol	Type	Description	Bonded to package
1	**SCL/INT**	Digital Inout PU[1] OD[2]	I2C clock input / interrupt output	Yes
2	**GND**	Ground	Ground.	
3	**GND**	Ground	Ground.	
4	**VCC**	Power	Power (2.5V-4.2V) Should be forced to 5V for EEPROM programming	
5	**GND**	Ground	Ground.	
6	**SDA**	Digital Inout PU[1] OD[2]	I2C data.	
-	**AMUX**	Analog Output	Test pad to monitor internal voltages in Test/Debug mode.	No
-	**INT**	Digital Output	Interrupt dedicated output.	
-	**VCCIO**	Power	Powers the digital I/Os. Can be connected to VCC if compatible with the I2C host controller.	Bonded to VCC pad on lead frame

Table 16: Pin list (DFN6)

(3) PD means weak internal Pulldown; PU means weak internal Pullup.
(4) OD means Open-Drain.