1. GENERAL DESCRIPTION

The SENIS® Fast Magnetic Angle Sensor (FAMAS) SENA2Dx is an integrated magnetic field sensor that allows the measurement of the rotation angle of the in-plane components of a magnetic field, such as that of a permanent magnet attached on-axis to a rotating shaft[1]. The co-integrated signal processing circuit represents a servo loop to track the external field which directly converts the angular position of the magnetic field to digital information. Thus, the angular position of the magnetic field, rotation direction, and angular velocity are available after less than 1 µs delay time. There are three modes of operation available - fast, balanced and high resolution – to offer optimal performance for the required application.

FEATURES:	TYPICAL APPLICATIONS:
▪ Contactless angle sensor 0–360° ▪ Hall-based principle with patented direct angle-to-digital conversion (no angle calculation necessary) ▪ Three selectable magnetic field strengths: low (20 mT), medium (100 mT) and high (400 mT) ▪ High magnetic fields of more than 500 mT do not cause damage to the sensor ▪ Small angle sensing volume of 100 x 100 x 10 µm^3 ▪ 12 bit representation of angle value, i.e. resolution 0.088° ▪ Fast response time, signal propagation delay < 1 µs ▪ Measures the direction, angle and rotation speed of the magnetic field, from DC up to 400 krpm ▪ On-chip offset, sensitivity and angle error correction ▪ On-chip temperature compensation of offset and sensitivity ▪ Non-volatile memory for permanent configuration and correction programming ▪ Interfaces: 4-wire SPI (5V), Quadrature interface with Index (ABZ), Commutation signals (UVW) ▪ Customer programming functions (SPI) • Set zero rot. position • Digital output format selection: ABZ or UVW • Selectable resolution from 8 to 12 bit • Angle error correction • UVW configurable for 2, 4, 6 and 8 pole magnets ▪ Low magnetic field threshold detection	▪ Absolute rotary position sensor ▪ Motor controlled applications • Robotic systems • DC brushless motors • Motor feedback/motion control • Rotational speed control ▪ Optical encoder replacement ▪ Potentiometer replacement ▪ High speed machining tools

[1] The angle sensing principle allows also for off-axis placement of the permanent magnet. This feature will be available soon.

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3. PACKAGE INFORMATION

The non-magnetic QFN28 package has a lead frame made of copper and the body material is a semiconductor molding epoxy. The FSV is about 0.75 mm below the surface of the package. Contact SENIS for details.

3.1 Dimensions

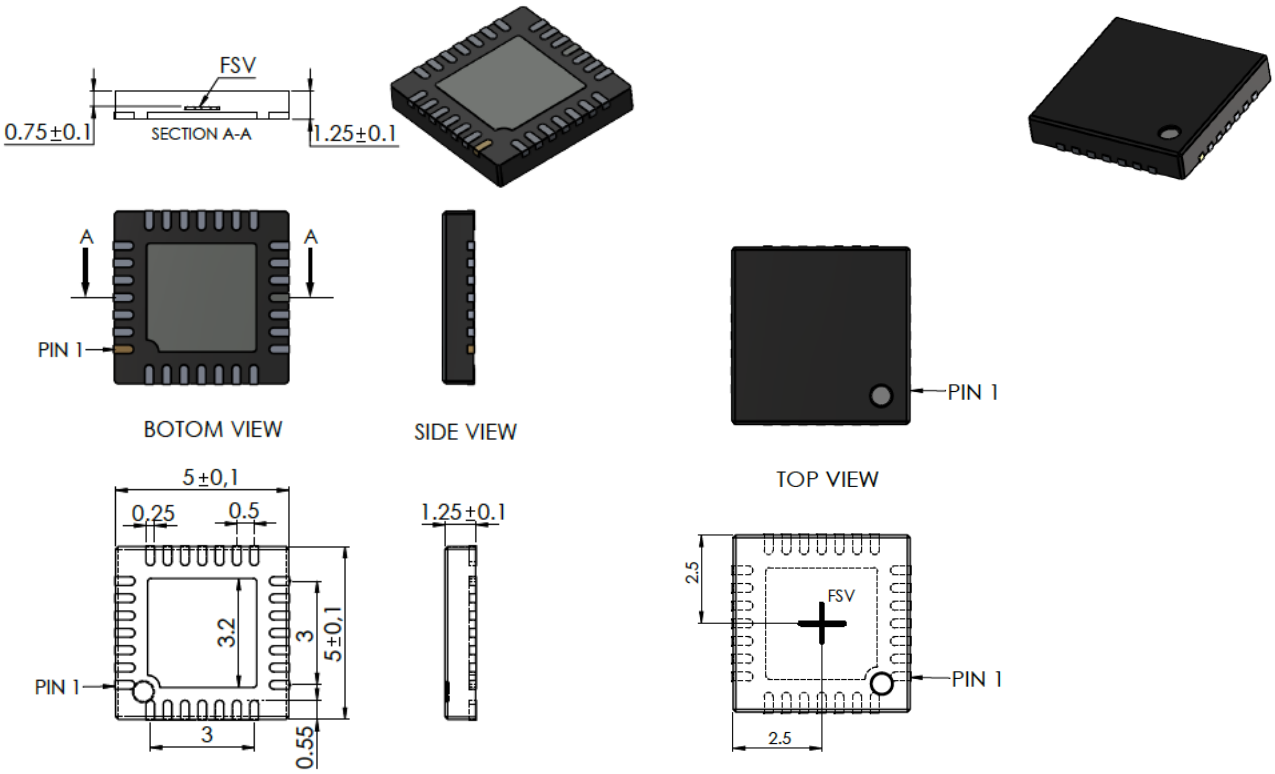

Figure 1: Dimensions of QFN 5x5 mm² package with 28 pins. The field sensitive volume (FSV) is located at the center of the package. Not to scale

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3.2 Pinout

Pin #	Symbol	Type	Direction	Description.
1	-	-	-	Not connected
2	-	-	-	Not connected
3	-	-	-	Not connected
4	-	-	-	Not connected
5	-	-	-	Not connected
6	-	-	-	Not connected
7	-	-	-	Not connected
8	VREF	Analog	Out	Bandgap reference voltage (+1.25V); bypass capacitor 100 nF to GNDA
9	VCM	Ground	Power	Virtual ground (+2.5V); bypass capacitor 100 nF to GNDA optional
10	GNDA	Supply	Power	Ground analog
11	VCCA	Supply	Power	Internal regulated analog supply voltage (4.5V); bypass capacitors 10µF and 100 nF to GNDA
12	VCC	Supply	Power	Main supply voltage (+5V); bypass capacitors 10µF and 100 nF to GNDA
13	TEST_EN	Digital	In	For internal use only; do not connect
14	TEST_DMUX	Digital	Out	For internal use only; do not connect
15	MCLK	Digital	In	SPI Master Clock
16	-	-	-	Not connected
17	-	-	-	Not connected
18	-	-	-	Not connected
19	-	-	-	Not connected
20	-	-	-	Not connected
21	SSB	Digital	In	SPI Chip (Slave) Select; active-low
22	MOSI	Digital	In	SPI Master Out Slave In
23	MISO	Digital	Out	SPI Master In Slave Out
24	VDD	Supply	Power	Internal regulated digital supply voltage (3.3V); bypass capacitors 10 µF and 100 nF to GNDD; Note: When programming the OTP, VDD should be driven by the host. A peak current of 100 mA should be expected.
25	GNDD	Supply	Power	Ground digital
26	Z/W	Digital	Out	Index signal Z/commutation signal W
27	B/V	Digital	Out	Quadrature signal B/commutation signal V
28	A/U	Digital	Out	Quadrature signal A/commutation signal U

Table 1: SENA2Dx pin list

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3.3 Magnetic Field Sensitivity

Figure 2 shows the QFN28 package and corresponding magnetic sensitivity axis with respect to pin 1.

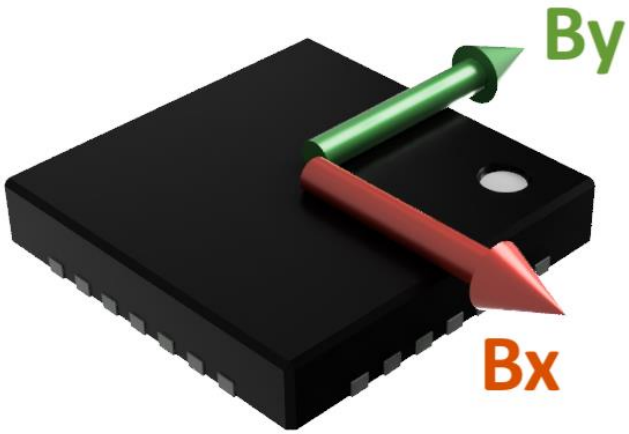

Figure 2: The two vertical Hall elements are sensitive in parallel to the chip/package surface.

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4. BLOCK DIAGRAM

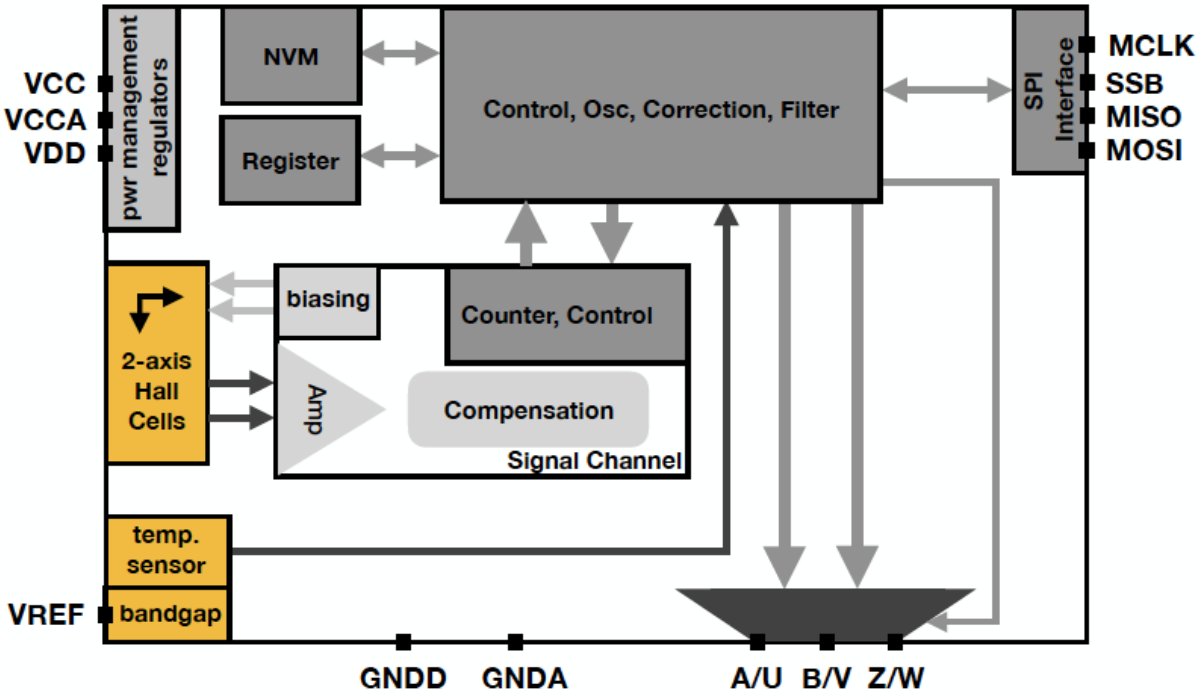

Figure 3: Block diagram of SENA2Dx

5. ABSOLUTE MAXIMUM RATINGS

Parameter	Min. Rating	Max. Rating	Unit
Power supply voltage VCC		7	V
Digital input voltage	-0.3	VCC+0.3	V
Shorted output current	-50	50	mA
Storage temperature	-50	150	°C
Operation temperature	-40	125	°C
Lead temperature, 10s soldering		220	°C
ESD protection at inputs, HBM	-2	2	kV
Magnetic field	-6	6	T

Table 2: Absolute maximal ratings

Note that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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6. GLOSSARY OF TERMS

Name, Acronym	Description
ABZ, AqB	Quadrature Encoder Channels, A, B Z (index; also referred to as I)
BW	Band Width
CPOL	Clock Polarity
CPHA	Clock Phase
DAC	Digital-to-Analog Converter
ENOB	Effective Number of Bits
ESD	Electrostatic Discharge
FSV	Field Sensitive Volume
HBM	Human-body model
MCLK	Master Clock
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Byte
NSD	Noise Spectral Density
NVM	Non-Volatile Memory
OTP	One-Time Programmable (Memory)
PWM	Pulse Width Modulation
RPM	Round Per Minute
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SSB	Slave Select Low-Active
UVW	Commutation Signals for Brushless DC Motors

Table 3: Glossary of terms

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7. ENCODER AND ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the given specifications and characteristics are typical values for V_{CC}=5V and a current consumption of 16 mA.

7.1 Power Domain

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max	
Power supply voltage	VCC	4.5	5	5.5	V
Current consumption	ICC		12	20	mA
Analog voltage regulator	VCCA		4.5		4.5
Digital voltage regulator	VDD		3.4		V
Reference voltage output	VREF		1.13		V
Virtual ground	VCM		2.42		V

Table 4: Typical characteristics of chip power domains

7.2 Digital Interface

Parameter	Symbol	Rating			Unit	Test Condition
		Min.	Typ.	Max		
High level input voltage	VIH	3	3.5	5	V	V_{CC}=5V
Low level input voltage	VIL	1	1.5	2	V	V_{CC}=5V
High level output voltage	VOH			VCC-0.3	V	I_{out}=4mA
Low level output voltage	VLH			0.3	V	I_{out}=4mA
Shorted output current	ISHORT	-50		50	mA	Output shorted to GND permanently
Input leakage current	ILEAK	-10		10	pA	
Input capacitance	CIN			5	pF	

Table 5: Electrical characteristics of digital IO

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7.3 Angle Sensor Performance

The overview in Table 6 shows the encoder ENOB vs. resolution, filter and spinning cycle selection. The shaded fields represent the predefined sensor operation modes High speed (8 bit res., 2 phase, no filter), Balanced (10 bit res., 2 phases, fast filter) and High precision (12 bit res., 4-phases, slow filter) chosen by defined by register FE_CONF (section 10.2.2).

Spinning cycle	Filter selection	No filter delay = <1 µs			Fast filter BW = 32 kHz; delay 5 µs			Slow filter BW = 8 kHz; delay 20 µs		
2-phase spinning	Sensor resolution sel. [bit]	10	9	8	10	10	10	12	11	10
	Encoder ENOB	9	8	7	10	10	9	12	11	10
	Max rotation speed [rpm]	50k	100k	>200k	50k	100k	200k	50k	100k	200k
4-phase spinning	Sensor resolution sel. [bit]	10	9	8	10	10	9	12	12	12
	Sensor ENOB [bit]	9	8	7	10	9	8	12	10	9
	Max rotation speed [rpm]	25k	50k	100k	25k	50k	100k	25k	50k	100k

Table 6: Overview of sensor performance for different operation modes and spinning cycles.

Parameter	Min.	Typ.	Max.	Unit
Sensor resolution	8	10	12	bit
AqB resolution	256	1024	4096	counts/revolution
AqB hysteresis		1		count

Table 7: Sensor characteristics.

Parameter	Min.	Typ.	Max.	Unit
Latency	< 1	5	20	µs
Relative angle error			0.08	°

Table 8: Sensor characteristics.

7.4 Hall Sensor Performance

Parameter	Min.	Typ.	Max.	Unit
Magnetic field sensitivity	20		300	mT
Field Sensitive Volume (FSV)		100 x 100 x 10		μm^3

Table 9: Electrical characteristics of digital IO

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8. SPI INTERFACE

The SENA2Dx is compatible with SPI mode 1, active-low chip (slave) select and fixed 8-bit length. This means, that clock polarity (CPOL) equals '0' and clock phase (CPHA) equals '1', i.e. data will be transferred on the falling edge of MCLK, while '0' is the idle or inactive state of MCLK. The SENA3Dx behaves always as slave of the SPI communication interface.

Parameter	Symbol	Min.	Max.	Unit
Clock period	Tcp	30		ns
Setup time from SSB low to MCLK high	Tsc	100		ns
Hold time from SSB high to MCLK low	Thc	100		ns
MOSI setup time to MCLK (1->0)	Tsi	5		ns
MOSI Hold time to MCLK (1->0)	Thi	0		ns
MISO propagation time from tri-state to logic (SSB=0)	Ttr2d		10	ns
MISO propagation time from logic to tri-state (SSB=1)	Td2tr		10	ns
MISO propagation time from MCLK (1->0)	Tdo		8	ns

Table 10: SPI timing parameter

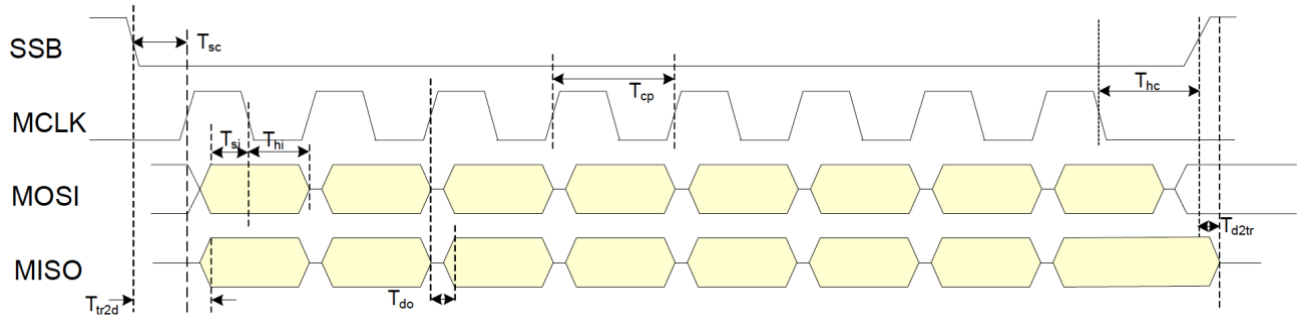

Figure 4: SPI timing parameter definitions

8.1 Register Read/Write Access

The access to the SPI interface is memory mapped and implemented as follows:
The first byte (8 bits) sent from the master (host; MOSI) represents a command word and includes a direction control bit (most significant bit): '0' for read and '1' for write access followed by a 7-bit address ADD (Figure 5 and Figure 6).

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8.1.1 Register Read Access

For a register read operation[2], the SENA3Dx responds (MISO) - by sending the most significant bit first - the data byte (Data[ADD]) from the provided address. The addressed data is available and valid after one byte delay, following the address byte. Multiple bytes can be read sequentially - from the provided address on - in a single SPI frame, which closes with the rising SSB signal.

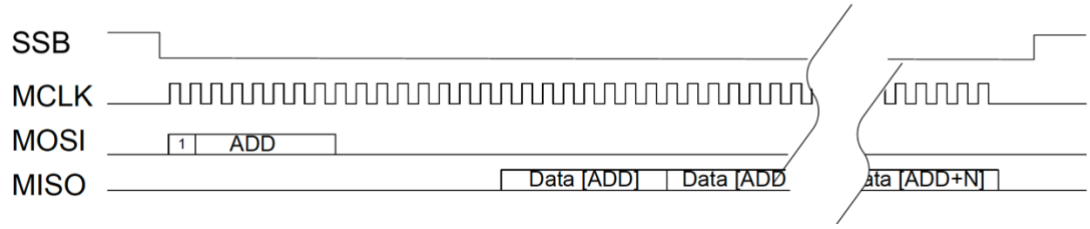

Figure 5: SPI communication for register read access timing diagram.

8.1.2 Register Write Access

The register write access starts with a leading (most significant bit) '0', followed by 7 address bits to conclude the first byte sent from the host (*Figure 6*). The second byte (or following) contains the data to write. Again, as mentioned for the register read access, also the write operation may be performed sequentially within one SPI frame for incremental addresses. Note that during the write process the MISO signal is unused, thus kept at '0'.

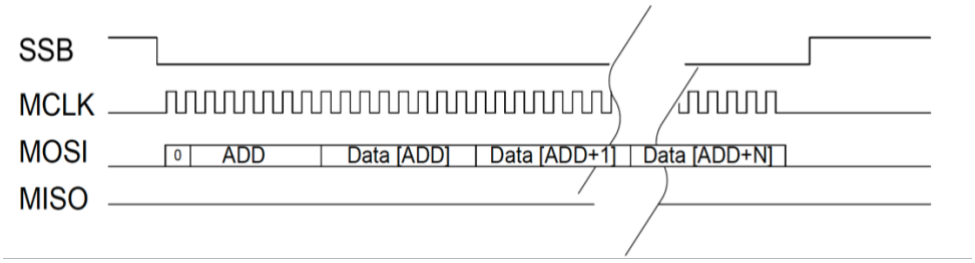

Figure 6: SPI Communication for register write access timing diagram

[2] In section 10.2.11 a different SPI communication scheme for read access is shown to get the angle and rotation data only.

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9. OTP ACCESS AND PROGRAMMING/FUSING

Once the user is content with the sensor settings and they should be written permanently to the non-volatile OTP memory, the fusing or burning procedure can be initiated. Note that during the fusing, the digital supply voltage VDD of sensor needs to be supplied externally using a decoupling capacitance of 10 µF to GND.
Only if the register OTP_CHECKSUM and OTP_KEY contain the right values (section 10.2.8), the OTP memory content will be loaded to the respective registers at power-up.

The two registers OTP_ACCESS1 and 2 (address 0x13 and 0x14), shown in Table 11 and detailed in section 10.2.10, are the interface to allow manual programming and read back of the OTP memory. The register OTP_ACCESS_EN (address 0x11) is used to enable (value 0xA0) the access to the OTP memory through OTP_ACCESS1 and 2. Actually, the register OTP_ACCESS_2 is used to encode the OTP address as follows:

OTP_ACCESS_2[2:0] = Bitadd, address bits within a byte
OTP_ACCESS_2[6:0] = Byteadd, address the corresponding byte from 0x00 to 0x0F (Table 12)

There is an SRAM buffer inside the OTP to buffer data that is loaded from the OTP.

0	0	1	1	1	0	0	1	**0x39**
0	0	1	1	1	0	0	0	**0x38**
0	1	0	0	0	1	0	0	**0x44**
0	1	0	0	0	0	0	0	**0x40**
unused	Comp_n	Ana_n	Anaburn_n	Burn_n	RW_clk	Load_p	Load_s	**Hex value**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
bit of OPT_ACCESS1 register								

Table 11: OTP_ACCESS1 register; address 0x13.

9.1 OTP Programming/ Write OTP

The OTP programming is entirely host controlled and to write data into the OTP memory, only the bits that are '1' need to be "burned". Note that the SRAM buffer is not involved in the OTP programming. The following pseudo code details the OTP programming procedure:

```
Set Reg 0x11 = 0xA0, enable access to write OTP
If (data_bit_to_burn == 1)
        Set Reg 0x14 = address of bit to burn (Byteadd<<3) + Bitadd
        Set Reg 0x13 = 0x40, prepare to burn, Comp_n high
        Set Reg 0x13 = 0x44, RW_clk high
        Set Reg 0x13 = 0x40, RW_clk low
        Set Reg 0x13 = 0x38, back to default, no burn
```


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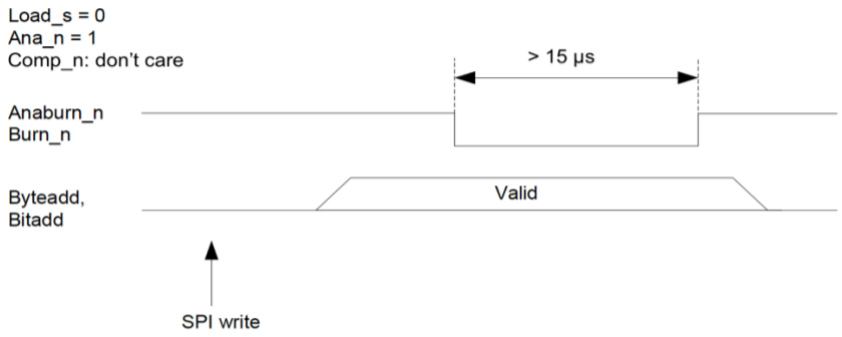

Figure 7: Timing diagram for OTP programming through OTP_ACEESS1 and 2 registers writing.

9.2 Read OTP to SRAM Buffer

When accessing the OTP SRAM buffer through SPI (address 0x40) the host should ensure that all bits of the OTP_ACCESS1 register are back to the default (address 0x13 to value 0x38).
To read back the OTP data, the following procedure should be used:

Set Reg 0x11 = 0xA0, enable access to write OTP
Reg 0x13 = 0x39, Load_s high
Reg 0x13 = 0x38, Load_s low
Read from Reg address 0x40 on the 16 bytes.

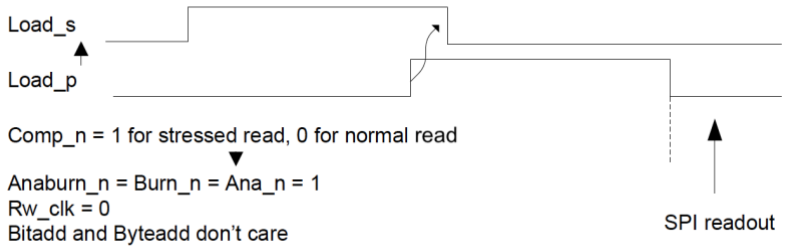

Figure 8: Timing diagram for OTP reading through OTP_ACEESS registers and SRAM buffer.

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9.3 Monitor Fuse Impedance of OTP

The fuse impedance the OTP data, the following procedure should be used:

Reg 0x13 = 0x01 or 0x39, toggle Load_s
Reg 0x13 = 0x00 or 0x38
Read from Reg 0x40 the 16 bytes.

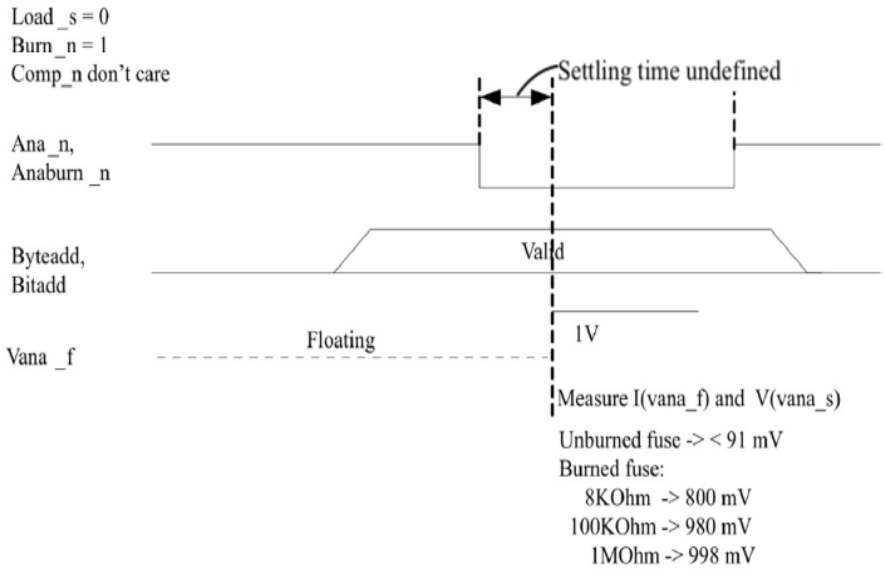

Figure 9: Timing diagram for OTP programming through OTP_ACEESS registers writing.

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10. REGISTERS

10.1 Register Map

Table 12 shows a list of all user relevant registers. Register addresses which are not shown in the list (e.g. 0x31 to 0xFF) must not be written, since they contain data essential for the ASIC operation. The default values detailed in the list are loaded to the registers at power-up if the EEPROM data is not activated (i.e. valid check sum and key present). Note that LSB and MSB are used here for least and most significant byte respectively. Register REG_0 to REG_7 control the spinning current state machine and the default values are the best possible settings, thus they should not be changed.

Register ID	Address	Default value	Mode	Meaning	NVM/OTP location
REG_0	0x00	16	R/W	Do not change	Yes
REG_1	0x01	18	R/W	Do not change	Yes
REG_2	0x02	19	R/W	Do not change	Yes
REG_3	0x03	17	R/W	Do not change	Yes
REG_4	0x04	57	R/W	Do not change	Yes
REG_5	0x05	60	R/W	Do not change	Yes
REG_6	0x06	0	R/W	Do not change	Yes
REG_7	0x07	0	R/W	Do not change	Yes
FE_CONF	0x08	2	R/W	Front-End control	Yes
G_COMP	0x09	136	R/W	Gain compensation for since & cosine signal path	Yes
DATA_CONF	0x0A	0	R/W	AqB control; data output configuration	Yes
E_COMP	0x0B	0	R/W	Sensor non-linearity error compensation.	Yes
OSC trim	0x0C	32	R/W	Oscillator trim data.	Yes
MODE	0x0D	3	R/W	Operation mode control & status	Yes
OTP_CHECKSUM[3]	0x0E	0	-	Valid checksum excepted	Yes
OTP_KEY[3]	0x0F	0	-	Register value should equal 0xA5 if OTP should be used	Yes

[3] Only if there is a valid checksum and the valid key present in the registers, the OTP content is being used. Note that the two values are written to the OTP and since only bit value '1' can be fused, the checksum and key may be only made invalid afterward.

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TEST	0x10	0	R/W	Do not change	No
OTP_ACCESS_EN	0x11	0	R/W	Enable access to OTP memory	No
STATUS	0x12	-	R/W	Sensor status register	No
OTP_ACCESS1	0x13	56	R/W	Manual control of OTP memory; control	No
OTP_ACCESS2	0x14	0	R/W	Manual control of OTP memory; addressing	No
TEST3	0x20	-	R	For internal use only	No
OTP_SRAM	0x40	0	R/W	The SRAM buffer is used to read data from the OTP memory	No
ROT_SPEED	0x7E	-	R	Rotation speed data reading	No
ANG_DATA	0x7F	-	R	Angle measurement data reading	No

Table 12: Overview register map and default settings.

10.2 Detailed Register Content

10.2.1 Spinning Phase Settings

The sequencer is configured by register values from address 0x00 to 0x07. The user should not change those values and if the data loading from the OTP memory is activated, the default values shown in Table 12 have to be used.

Register ID	Address	Mode	Bits	Meaning	Default
REG_0 to REG_7	0x00 to 0x07	R/W	7:0	Do not change	Table 12

Table 13: Registers for Hall element spinning current setting

10.2.2 Sensor Front-End Control

The SENA2Dx signal processing chain has several amplification stages, whereas three gain settings are selectable (Table 14) to adapt the sensor sensitivity and thus its linear operation range according to the magnitude of the applied magnetic field. Also, the user has the flexibility to change the encoder resolution directly and select a filter to adjust the effective sensor resolution.

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Permanent magnet field strength	Magnetic field range[4] [mT]	Sensitivity
high	400	low
moderate	100	medium
low	20	high

Table 14: Magnetic field strength selection and corresponding magnetic field measurement ranges.

Register ID	Address	Mode	Bits	Meaning	Default
FE_CONF	0x08	R/W	1:0	Magnetic field strength selection (sensitivity): '00' -> low '01' -> moderate '1x' -> high (default)	2
			3:2	Encoder resolution[5] selection: '00' -> 10 or 12 bit (12 bit if slow filter is selected) '01' -> 9 bit[6] '1x' -> 8 bit[7]	0
			4	Spinning cycle selection: '0' -> 4-phase '1' -> 2-phase	0
			5	Not used.	0
			7:6	Output filter data selection '0' -> No filter (10 bit max) '1' -> Fast filter (10 bit max) '2' -> Slow filter (12 bit only)	0

Table 15: Register settings for sensor front-end control

10.2.3 Sine, Cosine Channel Gain Correction Settings

The SENA2Dx has two vertical Hall elements – X, sine and Y, cosine component of the magnetic field – and their gain may be adapted independently to correct for or compensate mismatches.

Register ID	Address	Mode	Bits	Meaning	Default
G_COMP	0x09	R/W	3:0	Gain compensation for sine, X 0000 -> -1.5% 1000 -> 0% 1111 -> +1.5%	8
			7:4	Gain compensation for cosine, Y 0000 -> -1.5% 1000 -> 0% 1111 -> +1.5%	8

Table 16: Gain correction setting for sine and cosine channel

[4] The magnetic field ranges are not exact values since the device is not calibrated for this measurement.
[5] The number of bits is adjusted by removing the corresponding LSBs. MSB are filled with '0' in case the filter output is not wide enough.
[6] Sensor resolution is 9 bit regardless of filter selection
[7] Sensor resolution is 8 bit regardless of filter selection

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10.2.4 AqB/UVW Interface Control and Data Configuration

There are four different index mode options programmable (bit 1:0 of DATA_CONF register) for the AqB interface which are shown in Figure 10 to Figure 13. The index signal appears once per revolution and the user can select its gating.

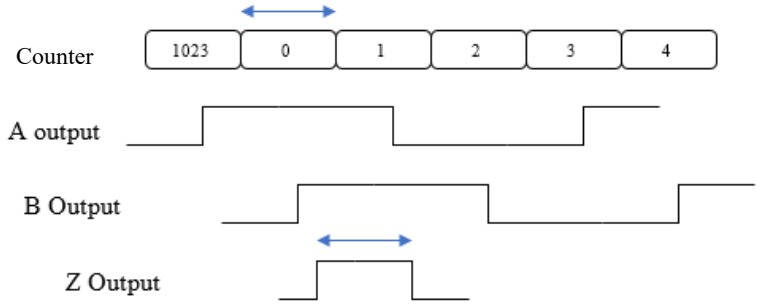

Figure 10: Ungated Index Option. The pulse width is the same as the counter data period.

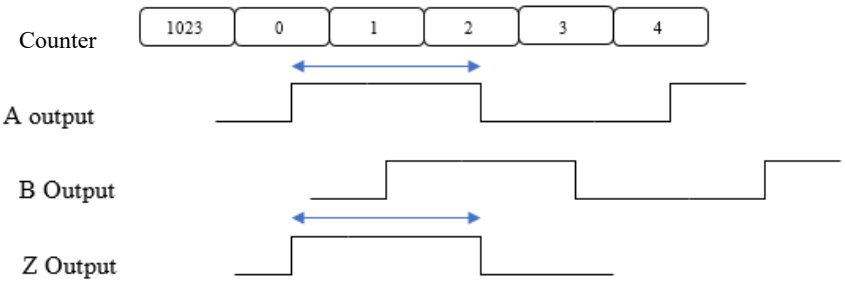

Figure 11: Index gated to A option. The pulse width is the same as the signal A period.

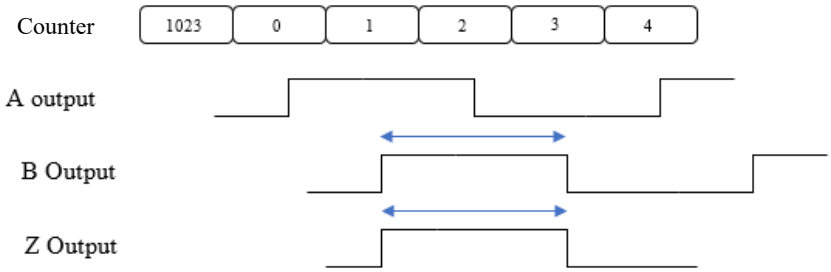

Figure 12: Index gated to B option. The pulse width is the same as the signal B period.

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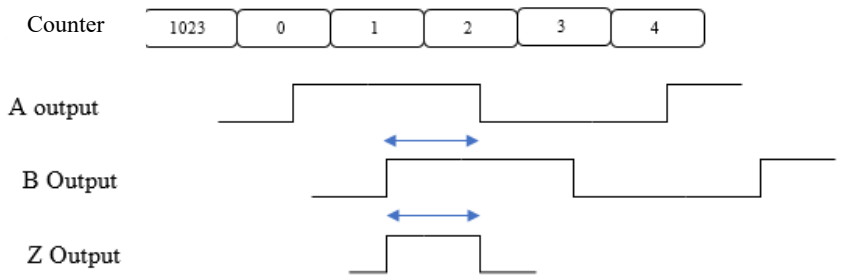

Figure 13: Index gated to A and B option. The pulse width equals the time when signal A and B are both high.

The motor commutation signals U, V and W can be adjusted according to the choice of a 1 to 4 pole pairs magnet. Figure 14 shows the UVW signals for the selection of 2 pole pairs (4 poles) during one revolution of the magnet and Table 17 details all four pole pair selection options.

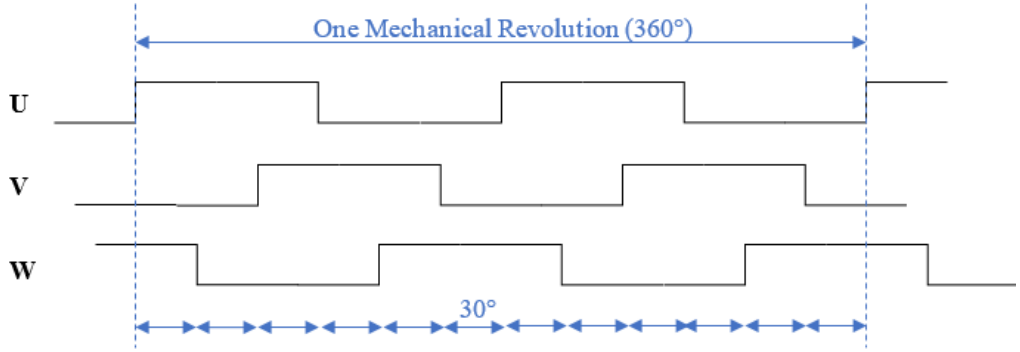

Figure 14: UVW Signals for 2 pole pair selection. One revolution is represented by 12 states with 30° each.

Magnet Selection - Pole Pairs	States/Revolution	°/State
1	6	60
2	12	30
3	18	20
4	24	15

Table 17: Magnet pole pair selection options and number of states and degrees per state.

Register ID	Address	Mode	Bits	Meaning	Default
DATA_CONF	0x0A	R/W	1:0	AqB index gating mode: 0-> Ungated: Z pulse lasts one data period 1-> Gated to A: Z pulse width equals signal A high time 2-> Gated to B: Z pulse width equals signal B high time 3-> Gated to A and B: a pulse width equals both A and B high time	0
			3:2	Number of pole pairs for UVW outputs: 0 -> 1 Pole pair (2 poles) 1 -> 2 Pole pair (4 poles) 2 -> 3 Pole pair (6 poles) 3 -> 4 Pole pair (8 poles)	0

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Register ID	Address	Mode	Bits	Meaning	Default
			5:4	Rotation speed measurement pre-scaler 0 -> 1 1 -> 8 2 -> 64 3 -> 512	0
			7:6	Not used	-

Table 18: Data configuration setting for the AqB/UVW interface and rotation speed measurement.

10.2.5 Sensor Non-Linearity Error Compensation

To improve the linearity of the sensor, an error compensation register is available to reduce the impact of poor magnet alignment with respect to the FSV. The error shows a sinusoidal pattern and there are three bits available to set the amplitude of the error compensation and one bit for the polarity of the correction signal which changes the phase by 180 degrees.

Register ID	Address	Mode	Bits	Meaning	Default
E_COMP	0x0B	R/W	2:0	Amplitude of compensation	0
			3	Polarity of compensation	0
			7:4	Not used	0

Table 19: Error compensation register settings.

10.2.6 Clock Frequency Settings

The nominal 20 MHz clock may be trimmed by the user within the range of 10 to 30 MHz.

Register ID	Address	Mode	Bits	Meaning	Default
OSC_TRIM	0x0C	R/W	5:0	Trim frequency by about: 300kHz /step	32
			7:6	Reserved	0

Table 20: Register for oscillator trimming

10.2.7 Operation Mode Selection and Sensor Status

The MODE register allows to select the operation mode of the encoder and choose the output interface. A monitoring circuit measures the magnetic field strength after power at power-up automatically. The measurement can be triggered by setting bit 7 to '1' and the result flag (weak magnetic field in XX) is updated. If the field magnitude is smaller than 20mT, the flag will be set to '1'.

Register ID	Address	Mode	Bits	Meaning	Default
MODE	0x0D	R/W	1:0	Select operation mode of the encoder: 00: User defined (use values in DATA_CONF register) 01: High speed (8 bit res., 2 phase, no filter) 10: Balanced (10 bit res., 2 phases, fast filter) 11: High precision (12 bit res., 4 phases, slow filter)	3
			2	Select digital output interface of the encoder 0 -> AqB 1 -> UVW	0
			4:3	Not used	0

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Register ID	Address	Mode	Bits	Meaning	Default
			5[8]	Reset zero angle position	0
			6[8]	Set current angle position as zero angle position	0
			7[8]	Trigger magnetic field measurement; flag update in STATUS register	0

Table 21: Register for operation mode settings.

10.2.8 OTP Checksum and Key Register

Registers from address 0x00 to 0x0F are used to calculate the checksum which is the two's complement sum of those registers, excluding OTP_CHECKSUM register value (address 0xE). That means, that the OTP memory content is valid if the sum of the whole OTP equals 0. The following procedure details the checksum calculation:

1: tmp_value = (sum of data from address 0x00 to 0x0D plus 0x0F) modulo 256
2: checksum = 256 – tmp_value

If the OTP_KEY register contains the valid key value 0xA5 and the OPT_CHECKSUM register has the valid checksum value, the OTP memory is unlocked and its data is loaded to the respective registers after power-up.

Register ID	Address	Mode	Bits	Meaning	Default
OTP_CHECKSUM	0x0E	-	7:0	Valid checksum: two's complement sum register value from address 0x00 to 0x0F excluding the OTP_CHECKSUM register value	0
OTP_KEY	0x0F	-	7:0	Register value 0xA5 unlocks the OTP together with a valid checksum in OTP_CHECKSUM register	0

Table 22: Register settings for OTP activation.

10.2.9 OTP_ACCESS_EN Register

To avoid accidental OTP access, the user has to write '101' to the OTP_ACCESS_EN[7:5] register. Any other value written will lead to normal register access but not OTP through registers OTP_ACCESS1 and 2. Only of the OTP access is enabled, operations explained in section **Error! Reference source not found.** and 10.2.10 are possible.

Register ID	Address	Mode	Bits	Meaning	Default
OTP_ACCESS_EN	0x11	R/W	4:0	Do not write	0
			7:5	Enable OTP access if value is 5 ('101')	0

Table 23: Register settings to enable access to the OTP memory through the OTP_ACCESS1 and 2 registers.

[8] After the operation is completed, this bit returns to '0'.

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10.2.10 OTP Access Register

The detailed procedure to access the OTP using the OTP_ACCESS registers is shown in chapter 9. Here, the single bits are explained which allow manual access to the OTP memory.

Register ID	Address	Mode	Bits	Meaning	Default
OTP_ACCESS1[9]	0x13	R/W	0	**Load_s** When set to 1, initiate data transfer from OTP fuses into local SRAM buffer. Should be deasserted when Load_p is asserted.	0
		R	1	**Load_p** Set to '1' by the OTP to acknowledge Load_s command. Set back to 0 to signal that the data inside the SRAM buffer is ready.	0
		R/W	2	**RW_clk** OTP clock A high pulse should be driven to either program the fuses, or perform an analog read (in both cases, bit and byte address defined in register OTP_ACCESS2). A minimum of 15 µs should be guaranteed for fusing.	0
			3	**Burn_n** Should be set to 0 in conjunction with Anaburn_n to burn the fuse selected bit, addressed by the OTP_ACCESS2 register.	1
			4	**Anaburn_n** See above	1
			5	**Ana_n** Should be set to 0 (while Burn_n and Anaburn_n are both 1).	1
			6	**Comp_n** 0 -> the data transfer from OTP to SRAM (triggered by Load_s rising edge) is done with a standard reference resistor. 1 -> the reference resistor is increased to verify proper fuse burning state.	0
			7	Not used.	0
OTP_ACCESS2[9]	0x14	R/W	2:0	**Bitadd** Data bit selection for fusing. 0=LSB … 7=MSB	0
			6:3	**Byteadd** Data byte address for burning or fuse impedance monitoring.	0
			7	Not used	0

Table 24: OTP access register settings to control OTP.

[9] If bit 7 to 5 of register OTP_ACCESS are not equal to '101', the write access to the register OPT_ACCESS1 and 2 is blocked, and both return default values.

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10.2.11 Rotation Speed and Angle Measurement Register

The data readout through SPI is somewhat different from normal register read access. The rotation speed and angle measurement are sent as 2-byte data and to ensure data consistency, a register access to ROT_SPEED and ANG_DATA requires that four data bytes (two data bytes, status byte, read checksum byte) have to be read in one SPI frame. Figure 15 shows the SPI timing diagram of a ROT_SPEED or ANG_DATA register read (most significant bit of the address is '1') access. Note the one byte delay between the MOSI read command and first valid MISO data byte (MSB).
The Checksum byte for the two registers read access is calculated by the following:

checksum_value = (sum of values: Data MSB, Data LSB , Status) modulo 256.

Thus, the user may verify if the received data is corrupt by verifying the checksum value.

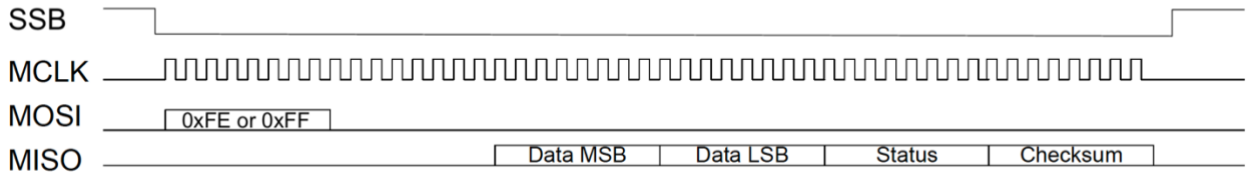

Figure 15: SPI timing diagram to read ROT_SPEED and ANG_DATA register data.

Calculation of rotation speed using the 16 bit counter value (ROT_SPEED register) and pre_scaler (DATA_CONF[5:4]):

8 bit mode: ω = 60/(counter*64*clock_period*pre_scaler) rpm
9 bit mode: ω = 60/(counter*128*clock_period*pre_scaler) rpm
10 bit mode: ω = 60/(counter*256*clock_period*pre_scaler) rpm
12 bit mode: ω = 60/(counter*1024*clock_period*pre_scaler) rpm

Note: Clock period is typ. 50 ns.

Register ID	Address	Mode	Meaning
ROT_SPEED	0x7E	R	16 bit rot. speed data, status byte, read checksum
ANG_DATA	0x7F	R	8 to 12 bit[10] angle data, status, read checksum

Table 25: Rotation speed and angle measurement data registers.

[10] If the angle data resolution is 9, 10 or 12 bit, the missing bits to fill one byte are zero padded.

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